

LCD Controller

Main features



- High Flexibility Frame Rates
- Drive up to 112 picture elements (pixels)
- Programmable duty and bias
- Low Power Waveform to reduce consumption
- Software selection between external and internal voltage source
- Interrupt driven refresh
- Contrast Control whatever power supply
- Blinking programmable pixels and frequency
- Unused segments and common pins can be used as I/O
- Full support of Low power modes



Frame ~30 Hz to
~100 Hz

A green starburst graphic with a dark blue outline is positioned to the right of the list. It contains the text 'Frame ~30 Hz to ~100 Hz' in a dark blue font.

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- The diagram illustrates the LCD clock divider circuit. It features three main functional blocks: a 16-bits Prescaler, a Clock MUX, and a Divide by 16 to 32 block. The input to the 16-bits Prescaler is RTCCLK/2. The output of the prescaler, CLKIN, is connected to the Clock MUX. The LCDCLK input is connected to the LCDFRQ block. The output of LCDFRQ is connected to the Clock MUX via the PS[3:0] signal. The Clock MUX also receives CLKIN/65596 as an input. The output of the Clock MUX is CLKps, which is then fed into the Divide by 16 to 32 block. The output of this block is CLKLCD. The DIV[3:0] signal, which is the output of the LCDFRQ block, is also connected to the Divide by 16 to 32 block.

- The frame frequency is obtained from the LCD frequency by dividing it by the number of active common terminals

$$f_{Frame} = f_{LCD} * duty$$

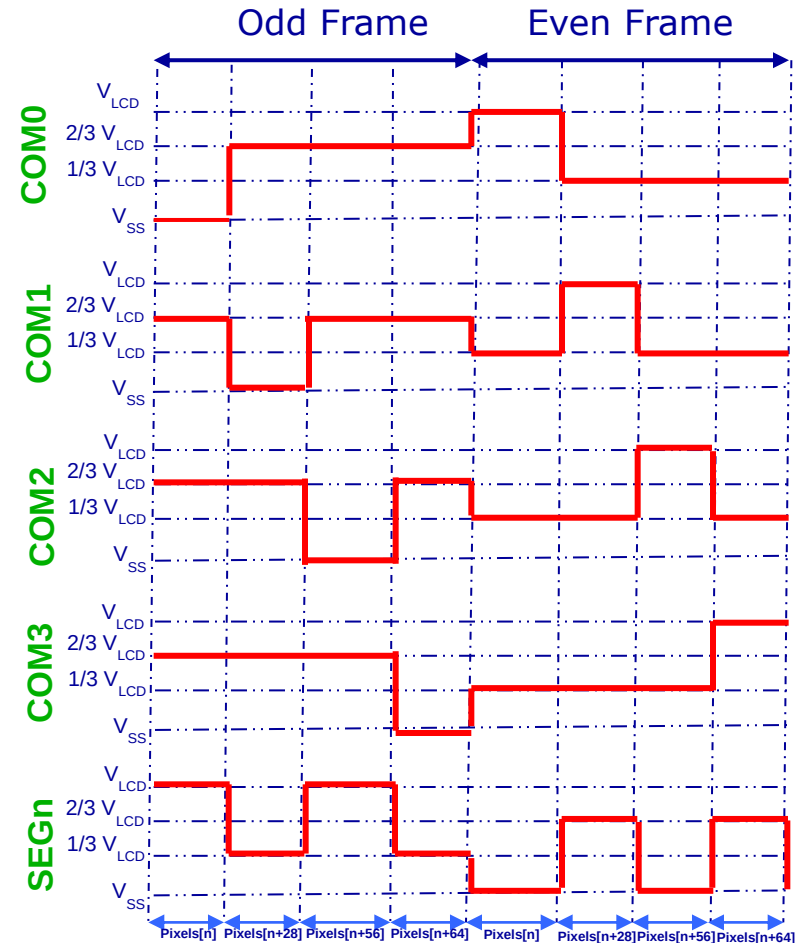
3

- Every common signal has identical waveforms but different phases
- The common has the maximum amplitude VLCD or VSS only in the corresponding phase of a frame cycle
- During the other phases, the signal amplitude is $\frac{1}{3}$ VLCD or $\frac{2}{3}$ VLCD in case of $\frac{1}{3}$ Bias and $\frac{1}{2}$ VLCD in case of $\frac{1}{2}$ Bias
- The first frame generated is the odd one followed by an even one
- Four Duty ratios can be selected: Static Duty, $\frac{1}{2}$ Duty, $\frac{1}{3}$ Duty or $\frac{1}{4}$ Duty
- Two modes can be selected: $\frac{1}{2}$ Bias or $\frac{1}{3}$ Bias

Common/Segment driver(2/3)



- The segment terminals are multiplexed and each of them controls four pixels
- A pixel is active if the corresponding segment line gets a maximum voltage opposite to the common
- Common signals are phase inverted in order to reduce EMI
- To activate pixels[n] connected to COM0, SEGn needs to be active during phase 0 of an odd frame and inactive during phase 0 of an even frame when COM0 is active
- To deactivate pixels[n+28] connected to COM1, SEGn needs to be inactive during the phase 1 of an odd frame and active during the Phase 1 of an even frame when COM1 is active



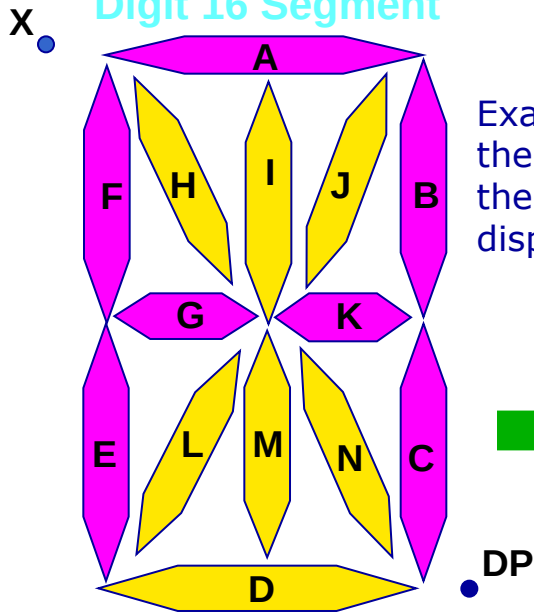
RAM refresh ↑

LCD RAM AREA ALWAYS ACCESSIBLE

Common/Segment driver(3/3)



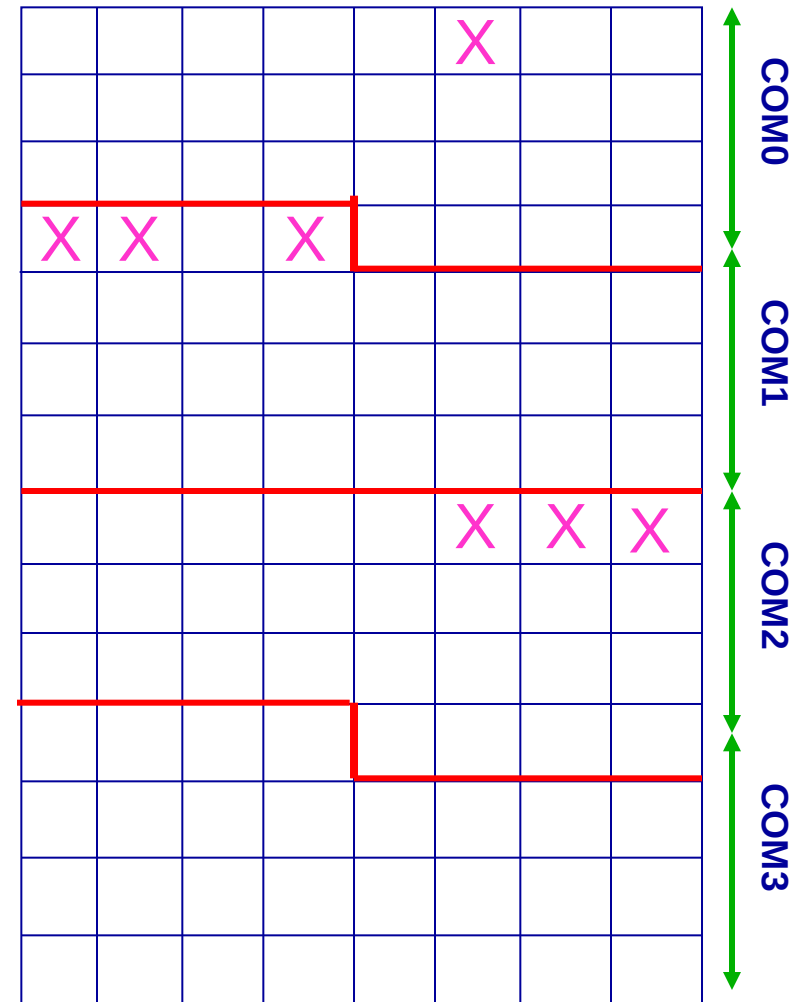
Digit 16 Segment



Example of Writing the character "A" on the Liquid crystal display first digit



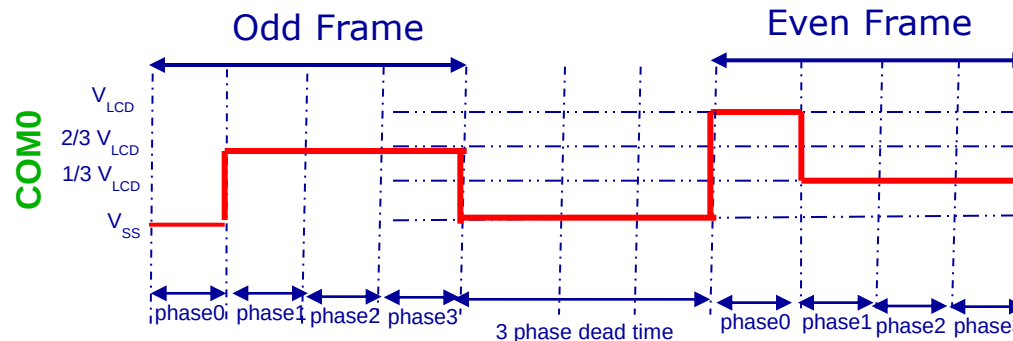
	COM0	COM1	COM2	COM3
SEG0	X	F	E	D
SEG1	I	J	K	N
SEG2	A	B	C	DP
SEG3	H	G	L	M
	4	D	7	0



RAM LCD

- The contrast can be adjusted using two different methods:

1- The contrast can be controlled by programming a dead time (up to 8 phase periods) between each couple of frames where the COM and SEG value is tied to V_{SS} in the same time.

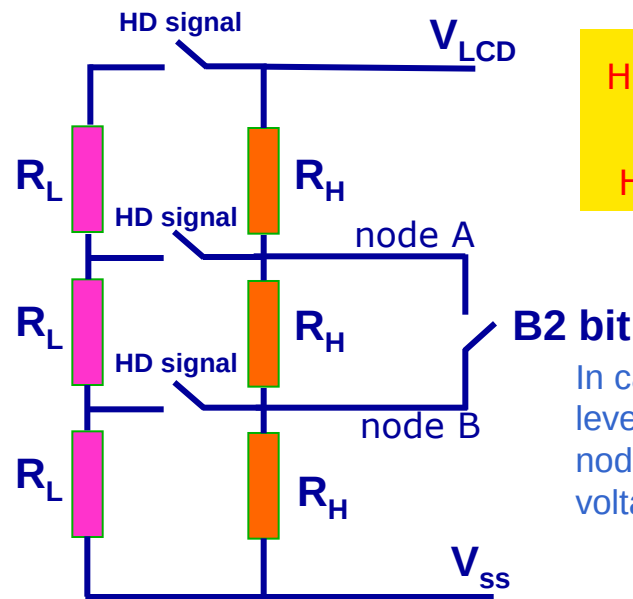


2- When using the internal voltage, the software can adjust VLCD between 2.6 V to 3.3 V in 8 steps

- The LCD voltage levels can be generated :
 - internally using an **internal booster** or externally using **VLCD voltage**
 - an **internal resistor** divider network which generates all VLCD intermediate voltages

The R_L and R_H resistive networks are used to increase the current during transitions and to reduce consumption in static state.

The time for which R_L is enabled through a HD signal can be configured using the pulse on duration bits.



HD (High Drive) signal
 $\neq$
HD (High Drive) Bit

In case of 1/2 Bias, one voltage level ($1/2 V_{LCD}$) is generated and node A voltage is equal to node B voltage and its value is $1/2 V_{LCD}$.

- The LCD remains active in wait, low power wait, low power run and active halt modes
- The LCD is not active in halt mode

- What is the LCD operation frequency range?

- Which clock sources can be used to provide the LCD clock ?

- Which values can be written on the LCD RAM registers to write the character “F” on the LCD first digit?

- How to adjust the contrast when using an external voltage source?

- How to adjust the contrast when using an external voltage source?

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