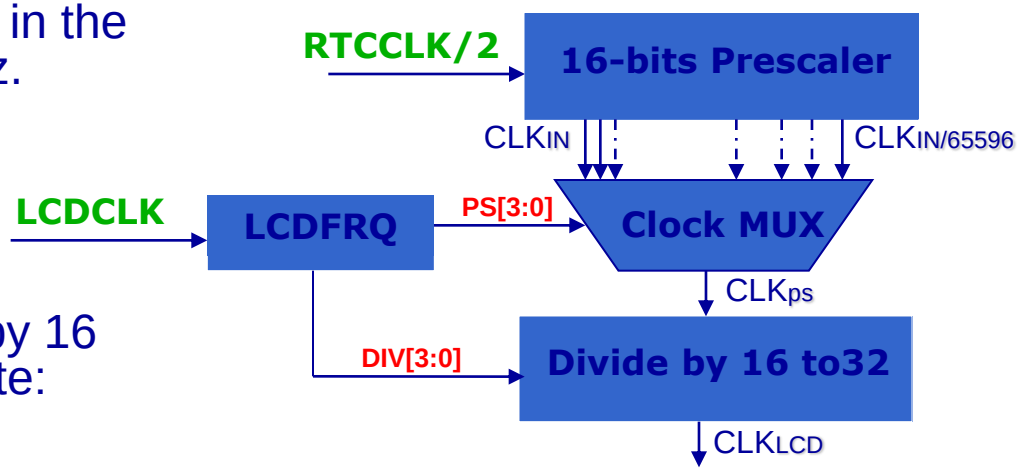
LCD Controller

Main features

- High Flexibility Frame Rates
- Drive up to 112 picture elements (pixels)
- Programmable duty and bias
- Low Power Waveform to reduce consumption
- Software selection between external and internal voltage source
- Interrupt driven refresh
- Contrast Control whatever power supply
- Blinking programmable pixels and frequency
- Unused segments and common pins can be used as I/O
- Full support of Low power modes

Frequency generator

- All clock sources can be used to provide the LCD clock
- The **CLKIN** input clock must be in the range of 16.384 kHz to 500 kHz.
- The **CLKIN** divided by $2^{PS[3:0]}$: **CLKps**
- The **CLKps** to be also divided by 16 to 31 to adjust the resolution rate: **CLKLCD**



$$f_{LCD} = \frac{f_{IN}}{2^{PS}(16 + DIV)}$$

- The frame frequency is obtained from the LCD frequency by dividing it by the number of active common terminals

$$f_{Frame} = f_{LCD} * duty$$

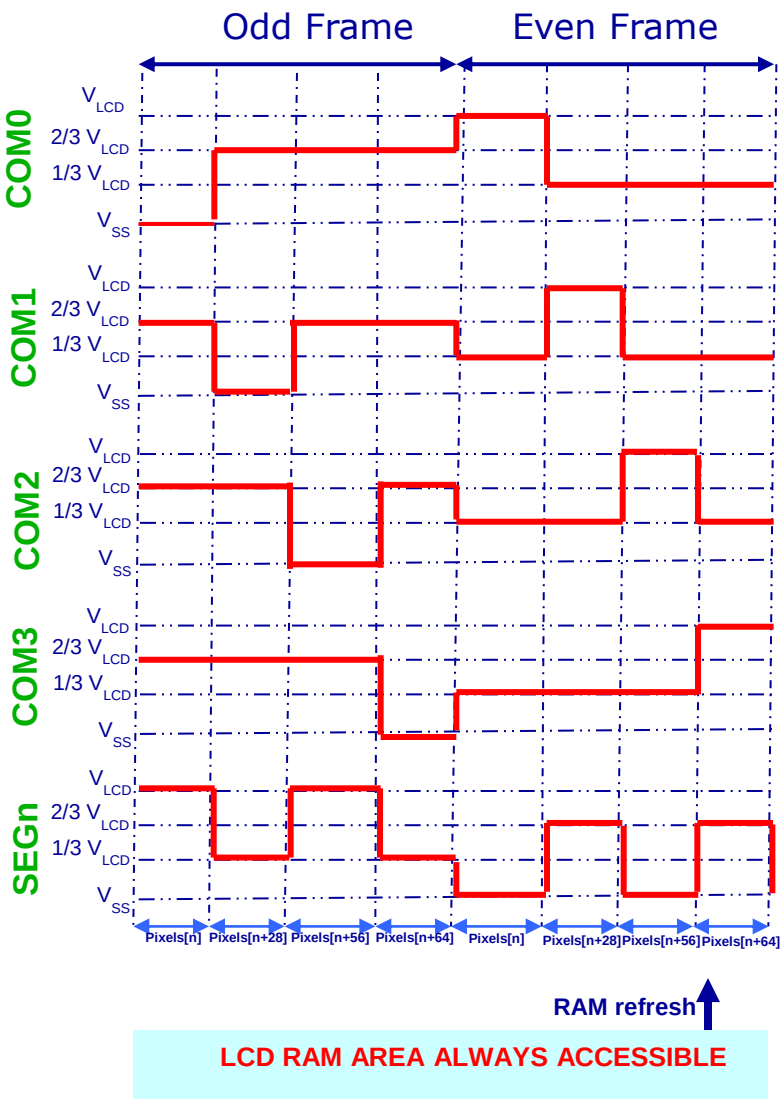
The frame frequency must be selected to be within a range of around ~30 Hz to ~100 Hz

Common/Segment driver(1/3)

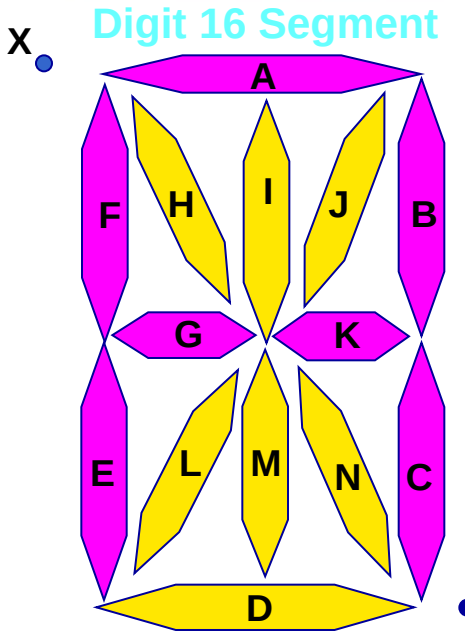
- Every common signal has identical waveforms but different phases
- The common has the maximum amplitude VLCD or VSS only in the corresponding phase of a frame cycle
- During the other phases, the signal amplitude is 1/3 VLCD or 2/3 VLCD in case of 1/3 Bias and 1/2 VLCD in case of 1/2 Bias
- The first frame generated is the odd one followed by an even one
- Four Duty ratios can be selected: Static Duty, 1/2 Duty, 1/3 Duty or 1/4 Duty
- Two modes can be selected: 1/2 Bias or 1/3 Bias

Common/Segment driver(2/3)

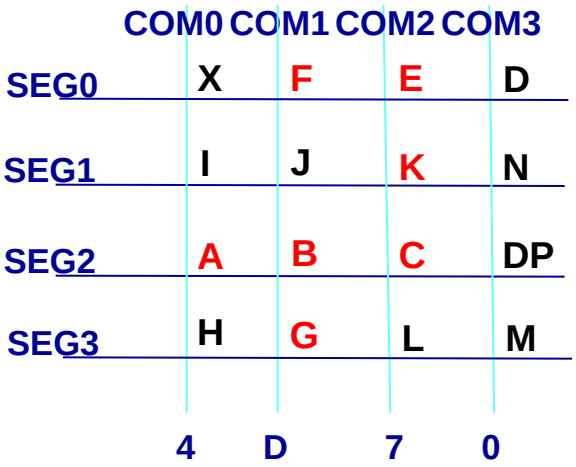
- The segment terminals are multiplexed and each of them controls four pixels
- A pixel is active if the corresponding segment line gets a maximum voltage opposite to the common
- Common signals are phase inverted in order to reduce EMI
- To activate pixels[n] connected to COM0, SEGn needs to be active during phase 0 of an odd frame and inactive during phase 0 of an even frame when COM0 is active
- To deactivate pixels[n+28] connected to COM1, SEGn needs to be inactive during the phase 1 of an odd frame and active during the Phase 1 of an even frame when COM1 is active

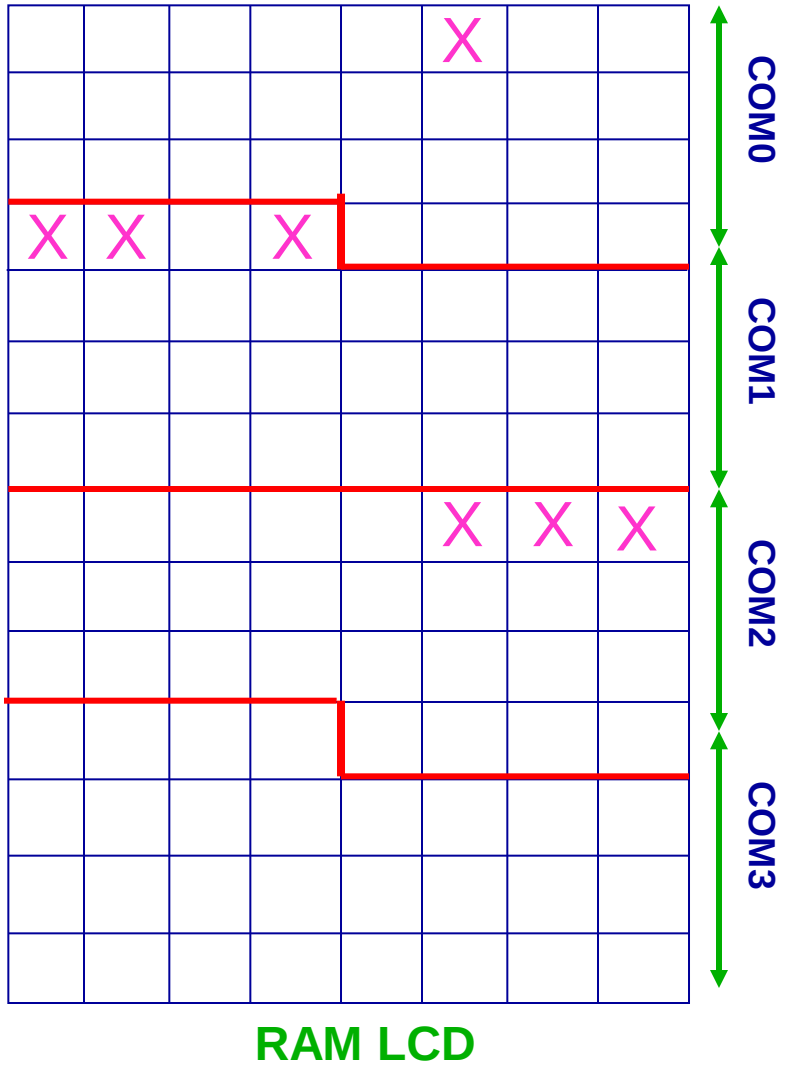


Common/Segment driver(3/3)



Example of Writing the character "A" on the Liquid crystal display first digit

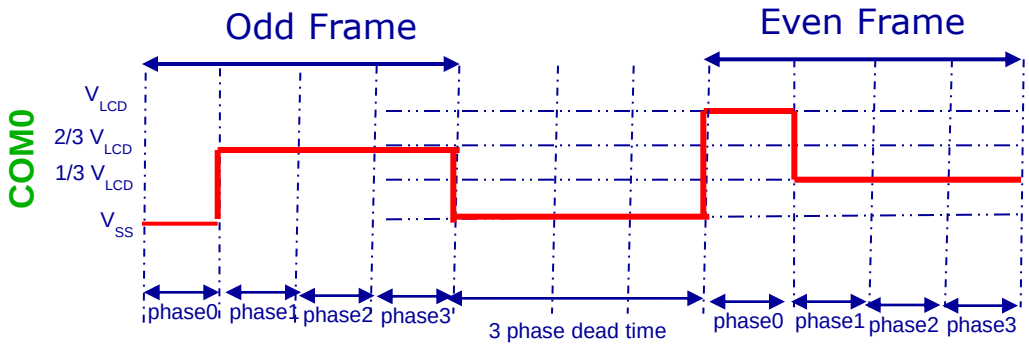




LCD Contrast Control

- The contrast can be adjusted using two different methods:

1- The contrast can be controlled by programming a dead time (up to 8 phase periods) between each couple of frames where the COM and SEG value is tied to Vss in the same time.



2- When using the internal voltage, the software can adjust VLCD between 2.6 V to 3.3 V in 8 steps

Power Conception

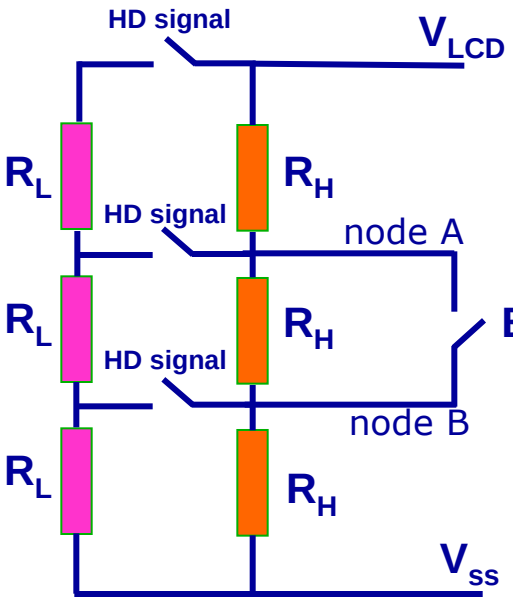
- The LCD voltage levels can be generated :

- internally using an **internal booster or** externally using **VLCD voltage**

- an **internal resistor** divider network which generates all VLCD intermediate voltages

The R_L and R_H resistive networks are used to increase the current during transitions and to reduce consumption in static state.

The time for which RL is enabled through a HD signal can be configured using the pulse on duration bits.



HD (High Drive) signal
≠
HD (High Drive) Bit

In case of 1/2 Bias, one voltage level (1/2 VLCD) is generated and node A voltage is equal to node B voltage and its value is 1/2 VLCD.

- The LCD remains active in wait, low power wait, low power run and active halt modes

- The LCD is not active in halt mode

Quiz

- What is the LCD operation frequency range?

  _____

- Which clock sources can be used to provide the LCD clock ?

  _____

- Which values can be written on the LCD RAM registers to write the character “F” on the LCD first digit?

  _____

- How to adjust the contrast when using an external voltage source?

  _____

- How to adjust the contrast when using an external voltage source?

  _____

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